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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,617	01/10/2002	Kyu-Hyoung Cho	5000-1-237	6501

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EXAMINER	
BELLO, AGUSTIN	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,617	CHO ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/30/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (U.S. Patent No. 5,864,416) in view of Chorey (U.S. Patent No. 6,163,709).

Regarding claim 1, Williams teaches an opto-electric converter (reference numeral 10 in Figure 1) for converting an input optical signal into an electrical signal, an amplifier circuit (reference numeral 20 in Figure 1) for amplifying the electrical signal; a bit rate-sensing circuit (inherent in reference numeral 50 in Figure 1 as described in column 3 line 67- column 4 line 5) connected to receive the amplified electrical signal for generating a sensing signal with a voltage level determined on the basis of a bit rate of the electrical signal; a bit rate-recognition circuit (inherent in reference numeral 50 in Figure 1 as described in column 3 line 67- column 4 line 5) for generating a recognition signal that is further amplified from the sensing signal, a clock/data

recovery circuit (reference numeral 50 in Figure 1) for reproducing a clock signal and data from the amplified electrical signal in accordance with a control signal (reference numeral 53 in Figure 1) and outputting the reproduced clock signal and data; and, a controller (reference numeral 100 in Figure 1) for determining a bit rate corresponding to a voltage level of the recognition signal by referring to a look-up table (column 4 lines 10-12) defining a predetermined relationship of the bit rate to the voltage level, and for providing the clock/data recovery circuit with the control signal (reference numeral 53 in Figure 1) representative of the bit rate. Williams differs from the claimed invention in that Williams fails to specifically teach that said bit rate-recognition circuit has a structure of providing an extended range of recognizable total input voltages by connecting a plurality of logarithm amplifiers in series, each of which logarithm amplifiers has a predetermined range of recognizable input voltage. However, such structures are well known in the art. Chorey, in the same field of detectors teaches such a structure (Figure 7). One skilled in the art would have been motivated to employ the structure taught by Chorey in the bit rate recognition circuit of Williams since such as structure is known to provide a dynamic range in excess of 50 dB (column 9 lines 1-3 of Chorey). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ the serial logarithm amplifier structure of Chorey in the bit rate-recognition circuit of Williams.

Regarding claim 2, the combination of references teaches a low-noise amplifier (reference numeral 20 in Figure 1 of Williams) for eliminating noise from the electrical signal outputted from the opto-electric converter (reference numeral 10 in Figure 1 of Williams) and for amplifying the noise-free electrical signal by a given amplification factor; and, a limiting

amplifier (reference numeral 90 in Figure 1) for re-amplifying the amplified electrical signal within a predetermined voltage level.

Regarding claim 3, the combination of references and Chorey in particular teaches a plurality of the logarithm amplifiers connected to sequentially amplify the sensing signal outputted from the bit rate-sensing circuit (Figure 7 of Chorey); a plurality of rectifiers (reference numeral 52, 54, 56, and 58 in Figure 7 of Chorey) respectively connected to one input of the respective logarithm amplifiers and to one output of at least one said logarithm amplifier, for rectifying the sensing signal inputted thereto; and, an adder (reference numeral 60 in Figure 1) connected to provide the sum of output signals of the plurality of rectifiers.

Regarding claim 4, the combination of references and Williams in particular teaches a phase-locked loop circuit (column 4 lines 1-2) for generating a reference clock signal in accordance with the control circuit provided by the controller (reference numeral 100 in Figure 1); and, at least one flip-flop (inherent in the clock/data recovery circuit 50 in Figure 1) connected to reproduce a clock signal (reference numeral 51 in Figure 1) and data (reference numeral 52 in Figure 1), in accordance with the reference clock signal, from the amplified electrical signal supplied from the amplifier circuit (reference numeral 95, 96 in Figure 1).

Regarding claim 6, the combination of references and Williams in particular teaches that the controller comprises a memory for storing a look-up table (column 4 lines 10-12) indicating a predetermined data set of the bit rate to the voltage level.

Regarding claim 7, Williams teaches a photodiode (reference numeral 10 in Figure 1).

Allowable Subject Matter

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 2/28/05 have been fully considered but they are not persuasive.

6. In response to applicant's argument that the combination of references fails to meet the limitations of the claimed invention and specifically fails to teach how each of the elements is used (e.g. a controller ***for*** ...), a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). In this case, the examiner has provided Williams which teaches every element recited with the exception of the internal structure of the bit rate-sensing circuit, for which the examiner relies on Chorey. Given that the claim language fails to provide any structural difference between the claimed elements and that of the prior art and seeks only to differentiate the claimed elements from those of the prior art by reciting how the elements are used or what they provide, the examiner has determined that the cited references when combined

meet the structural, and therefore, the intended uses of the elements recited in the claimed invention.

7. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

8. In response to applicant's argument that Chorey is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Chorey and Williams are directed in general to the field of communications and specifically to detectors of communication signals. Contrary to the applicant's assertions, the examiner has not considered the detector of Chorey as an optical detector.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AB

A. Bello

AGUSTIN BELLO
PRIMARY EXAMINER